Test Conditions for various vector groups commonly under use are listed along with pictorial representation. Assuming the reader has sufficient exposure to transformer winding connections.

Transformer Vector Group Test conditions

YNd1, YNd11, Dyn11, YNyn0 and more

Pandian

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Introduction

In transformers the interconnection of the coils and the phase angle between the primary and secondary side are denoted by standard form. Transformers with similar connections and phase shift are grouped under a Vector group.

Standard notations to denote the connection are listed below

	Connection	Notation
HV Winding	Star	Y
	Delta	D
	Neutral	N
	Zig Zag	Z
	Single Phase	I
LV Winding	Star	y
	Delta	d
	Zig Zag	z
	Neutral	n
	Single Phase	i

The phase shift between the primary and secondary side are denoted in the form of Clock Position. Taking HV side as the reference (i.e. 12 o Clock position) phase shift of the LV side is mentioned in numerical values in multiples of 30°

0 denotes 0°, 1 denotes 30°, 6 denotes 180° and so on. In special transformer where the phase shift is not in multiples of 30° particularly for the isolation transformer incorporated to reduce the harmonics, directly the phase angle is been mentioned by the manufacturers

To carry out the Vector Group test one should establish the electrical connection between Primary and Secondary since the separate winding transformers are inductively coupled whereas the auto transformers are electrically coupled and so no need for latter.

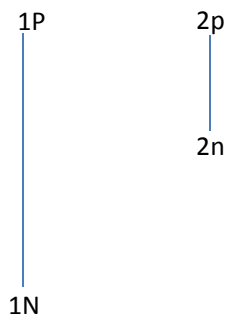
After establishing the electrical connection between two windings under test, voltage may be applied in either of the winding preferably in the HV side as it is safe and the voltage measured between the various terminals will be indicative to ensure the phase shift. Testing Engineer should derive at least three conditions to compare, add and or equate the particular set of voltage to be measured. These conditions should be in such way to ensure the phase shift and phase sequence.

Usually 1U and 2u are connected but it is not necessarily to be so, Testing Engineer can choose by his/her own choice and the conditions shall be derived accordingly.

If the derived conditions are satisfied the vector shall be confirmed.

Ii0

- Connect 1P and 2p
- Keep the neutral(1N & 2n)l floating
- Apply Voltage in HV side

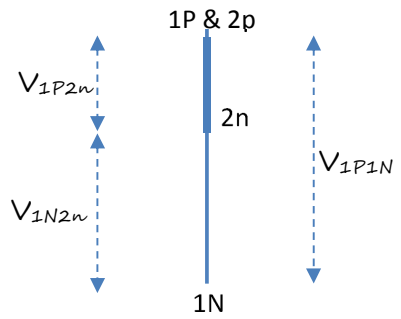


Condition

Measure Voltage between

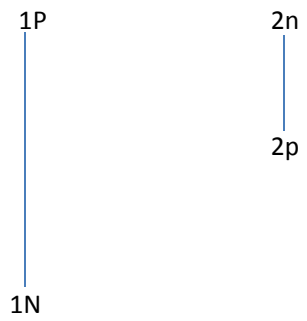
1. 1P and 2n (V_{1P2n})
2. 2n and 1N (V_{2n1N})
3. 1P and 1N (V_{1P1N})

$\mathbf{V_{1P2n} + V_{2n1N} = V_{1P1N}}$



Ii6

- Connect 1P and 2p
- Keep the neutral(1N & 2n)l floating
- Apply Voltage in HV side

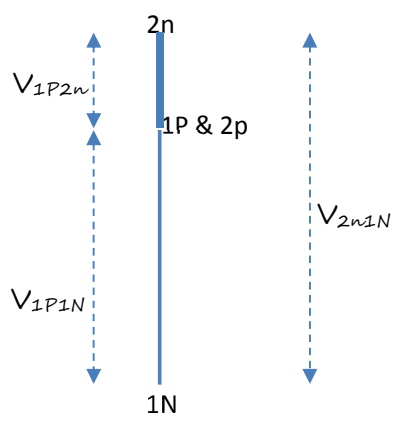


Condition

Measure Voltage between

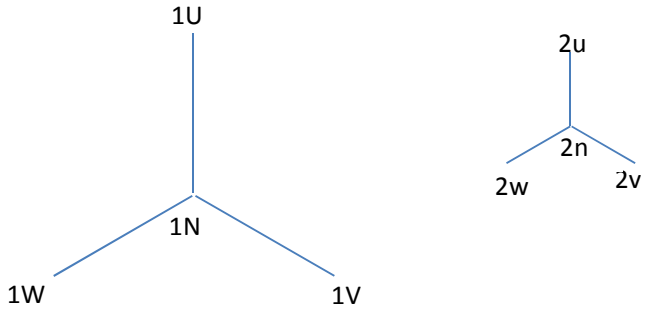
1. 1P and 2n (V_{1P2n})
2. 2n and 1N (V_{2n1N})
3. 1P and 1N (V_{1P1N})

$\mathbf{V_{1P2n} + V_{1P1N} = V_{2n1N}}$



YNyn0

- Connect 1U and 2u
- Keep the neutral floating
- Apply 3Φ Voltage in HV side

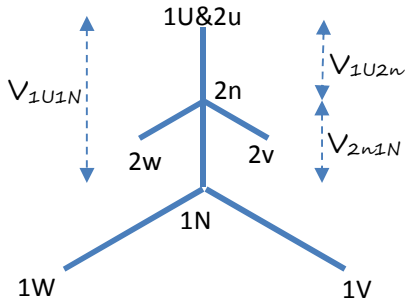


Condition – 1

Measure Voltage between

1. 1U and 2n (V_{1U2n})
2. 2n and 1N (V_{2n1N})
3. 1U and 1N (V_{1U1N})

$\mathbf{V_{1U2n} + V_{2n1N} = V_{1U1N}}$

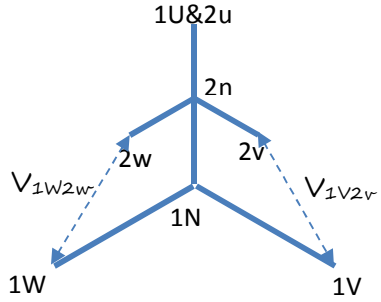


Condition – 2

Measure Voltage between

1. 1W and 2w (V_{1W2w})
2. 1V and 2v (V_{1V2v})

$\mathbf{V_{1W2w} = V_{1V2v}}$

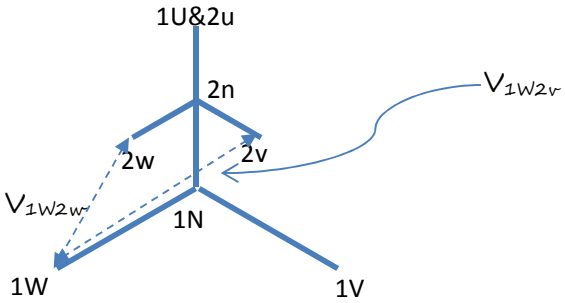


Condition – 3

Measure Voltage between

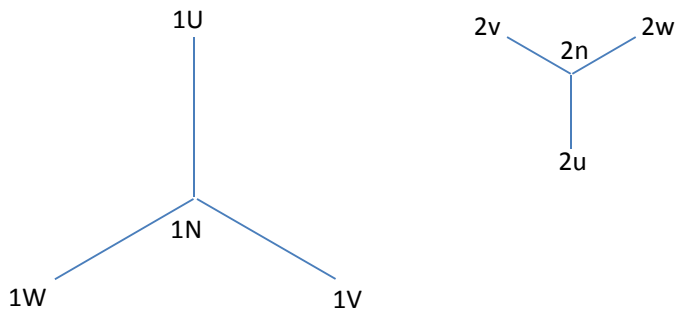
1. 1W and 2w (V_{1W2w})
2. 1W and 2v (V_{1V2v})

$\mathbf{V_{1W2w} < V_{1w2v}}$



YNyn6

- Connect 1U and 2u
- Keep the neutral floating
- Apply 3Φ Voltage in HV side

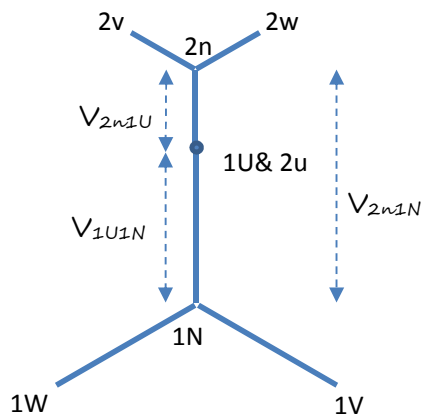


Condition – 1

Measure Voltage between

1. 1U and 2n (V_{2n1U})
2. 2n and 1N (V_{2n1N})
3. 1U and 1N (V_{1U1N})

$\mathbf{V_{2n1U} + V_{1U1N} = V_{2n1N}}$

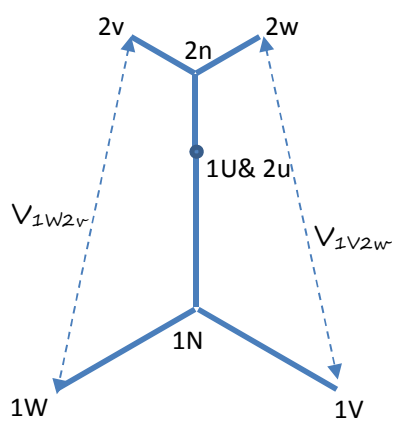


Condition – 2

Measure Voltage between

1. 1W and 2v (V_{1W2v})
2. 1V and 2w (V_{1V2w})

$\mathbf{V_{1W2v} = V_{1V2w}}$



1. Ensure only one terminal of HV and one terminal of LV is connected together
2. Ensure the additive voltage does not exceeds the safe limit

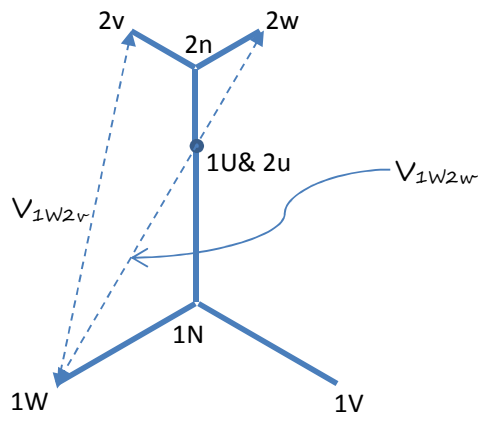
YNyn6...(contd)

Condition – 3

Measure Voltage between

1. 1W and 2v (V_{1W2v})
2. 1W and 2w (V_{1w2w})

V_{1W2w} > V_{1w2v}

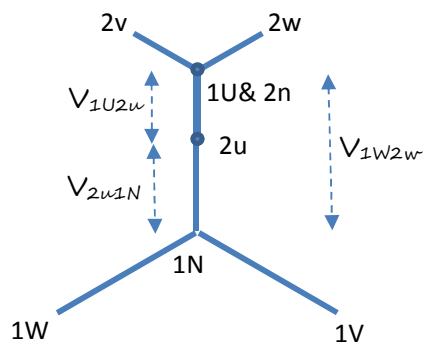


*By connecting 1U and 2u the Voltage V_{1W2w} may be high, hence the author feels comfortable to connect 1U and 2n. Then the Condition – 1 changes as follows and the Conditions – 2 & 3 remains unchanged

Measure Voltage between

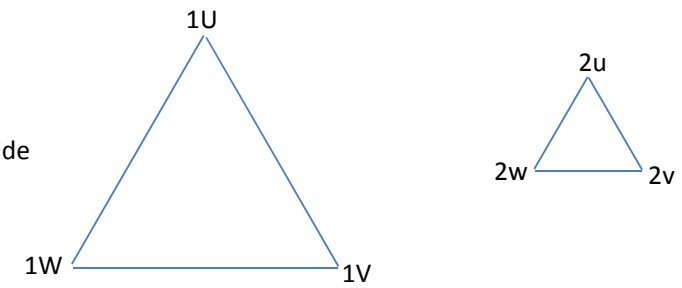
1. 1U and 2u (V_{1U2u})
2. 2u and 1N (V_{2u1N})
3. 1U and 1N (V_{1U1N})

$V_{1U2u} + V_{2u1N} = V_{1U1N}$



Dd0

- Connect 1U and 2u
- Apply 3Φ Voltage in HV side

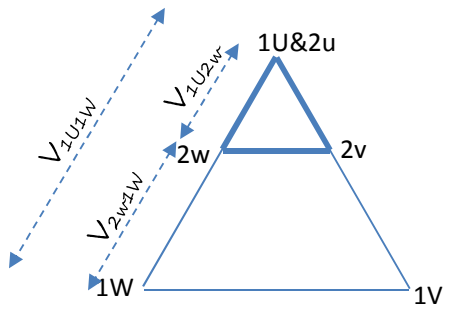


Condition – 1

Measure Voltage between

1. 1U and 2w (V_{1U2w})
2. 2w and 1W (V_{2w1W})
3. 1U and 1W (V_{1U1W})

$\mathbf{V_{1U2w} + V_{2w1W} = V_{1U1W}}$

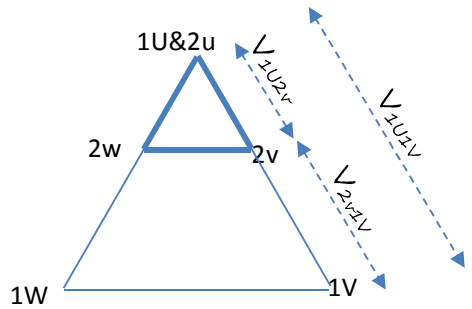


Condition – 2

Measure Voltage between

1. 1U and 2v (V_{1U2v})
2. 2v and 1V (V_{2v1V})
3. 1U and 1V (V_{1U1V})

$\mathbf{V_{1U2v} + V_{2v1V} = V_{1U1V}}$

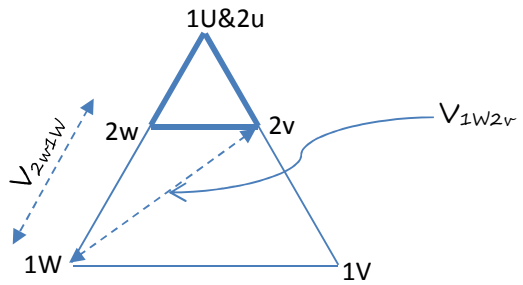


Condition – 3

Measure Voltage between

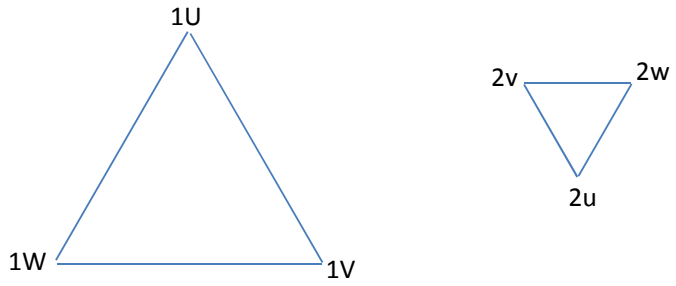
1. 1W and 2v (V_{1W2v})
2. 1W and 2w (V_{1w2w})

$\mathbf{V_{1W2w} < V_{1w2v}}$



Dd6

- Connect 1U and 2u
- Apply 3Φ Voltage in HV side

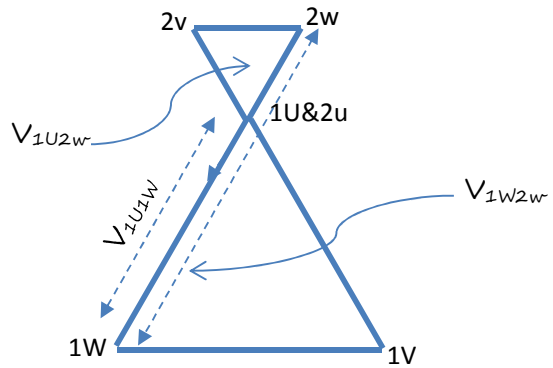


Condition – 1

Measure Voltage between

1. 1U and 2w (V_{1U2w})
2. 2w and 1W (V_{1W2w})
3. 1U and 1W (V_{1U1W})

$V_{1U1W} + V_{1U2w} = V_{1W2w}$

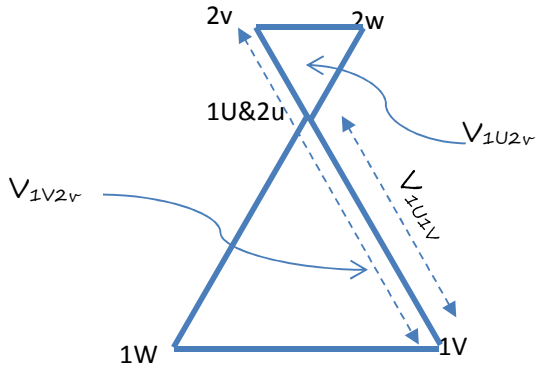


Condition – 2

Measure Voltage between

1. 1U and 2v (V_{1U2v})
2. 2v and 1V (V_{1V2v})
3. 1U and 1V (V_{1U1V})

$V_{1U1V} + V_{1U2v} = V_{1V2v}$



1. Ensure only one terminal of HV and one terminal of LV is connected together
2. Ensure the additive voltage does not exceeds the safe limit

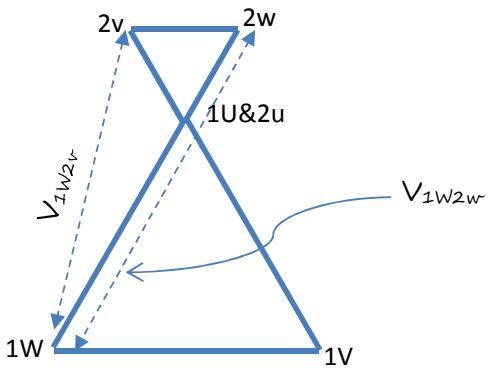
Dd6…(contd)

Condition – 3

Measure Voltage between

1. 1W and 2v (V_{1W2v})
2. 1W and 2w (V_{1w2w})

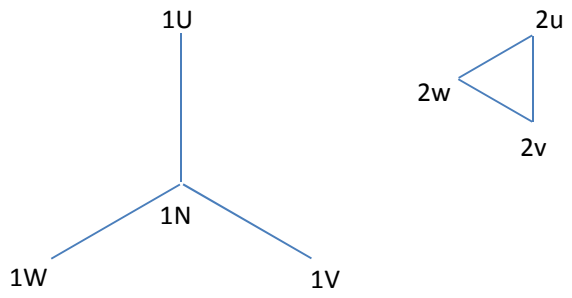
V_{1W2w} > V_{1w2v}



*By connecting 1U and 2u the Voltage V_{1W2w} may be high, hence the author feels comfortable to connect 1U and 2v and conditions shall be derived accordingly.

YNd1

- Connect 1U and 2u
- Keep the neutral floating
- Apply 3Φ Voltage in HV side

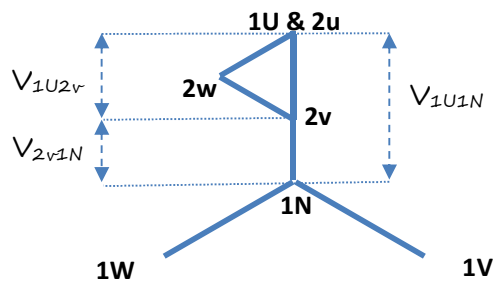


Condition - 1

Measure Voltage between

1. 1U and 2v (V_{1U2v})
2. 2v and 1N (V_{2v1N})
3. 1U and 1N (V_{1U1N})

$\mathbf{V_{1U2v} + V_{2v1N} = V_{1U1N}}$

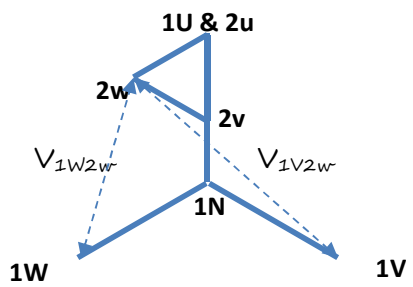


Condition – 2

Measure Voltage between

1. 1W and 2w (V_{1W2w})
2. 1V and 2w (V_{1V2w})

$\mathbf{V_{1W2w} < V_{1V2w}}$

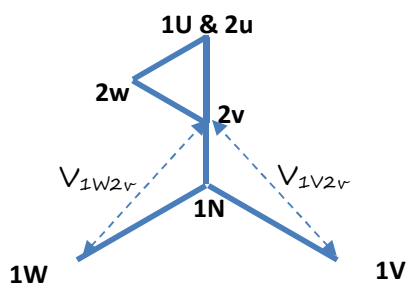


Condition – 3

Measure Voltage between

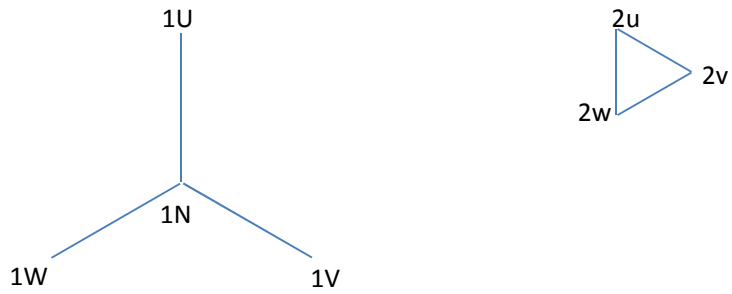
1. 1W and 2v (V_{1W2V})
2. 1V and 2v (V_{1V2v})

$\mathbf{V_{1W2V} = V_{1V2v}}$



YNd11

- Connect 1U and 2u
- Keep the neutral floating
- Apply 3Φ Voltage in HV side

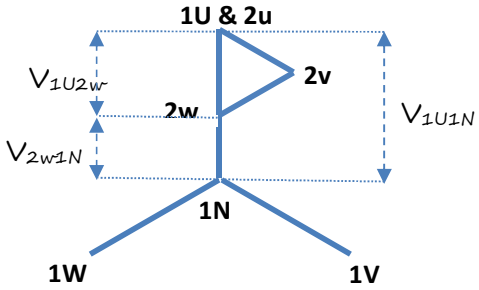


Condition - 1

Measure Voltage between

1. 1U and 2w (V_{1U2w})
2. 2w and 1N (V_{2w1N})
3. 1U and 1N (V_{1U1N})

$\mathbf{V_{1U2w} + V_{2w1N} = V_{1U1N}}$

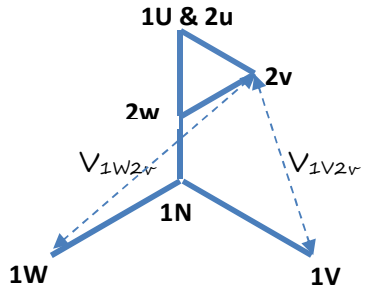


Condition - 2

Measure Voltage between

1. 1W and 2v (V_{1W2v})
2. 1V and 2v (V_{1V2v})

$\mathbf{V_{1W2v} > V_{1V2v}}$

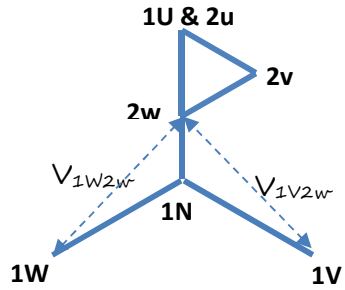


Condition -3

Measure Voltage between

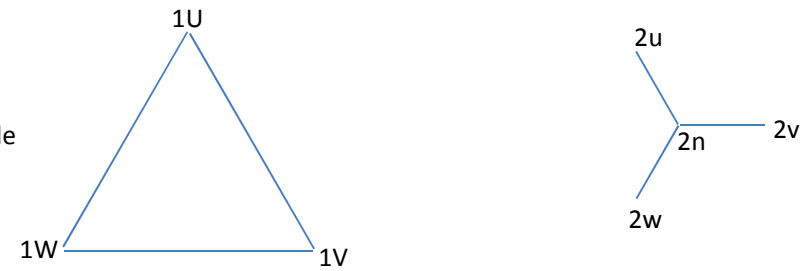
1. 1W and 2w (V_{1W2w})
2. 1V and 2w (V_{1V2w})

$\mathbf{V_{1W2w} = V_{1V2w}}$



Dyn11

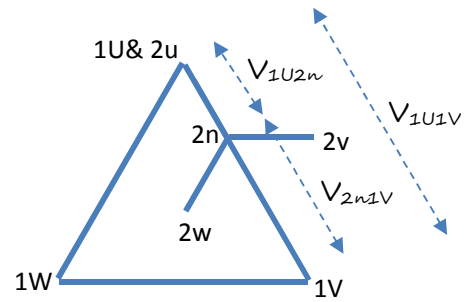
- Connect 1U and 2u
- Keep the neutral floating
- Apply 3Φ Voltage in HV side



Condition - 1

Measure Voltage between

1. 1U and 2n (V_{1U2n})
2. 2n and 1V (V_{2n1V})
3. 1U and 1V (V_{1U1V})

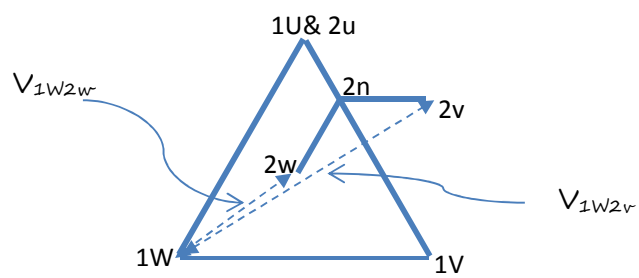


$\mathbf{V_{1U2n} + V_{2n1V} = V_{1U1V}}$

Condition - 2

Measure Voltage between

1. 1W and 2v (V_{1W2v})
2. 1W and 2w (V_{1W2w})

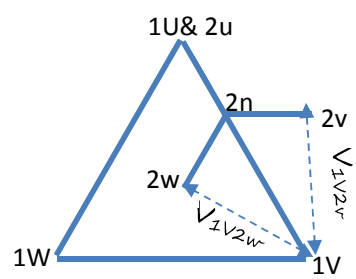


$\mathbf{V_{1W2v} > V_{1W2w}}$

Condition -3

Measure Voltage between

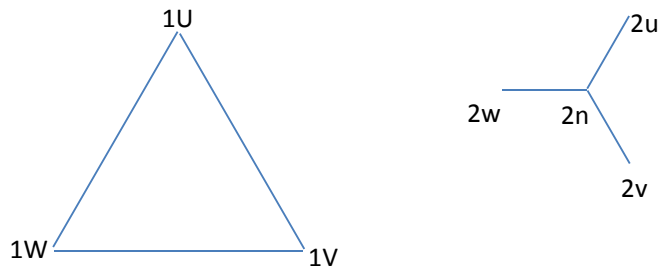
1. 1V and 2v (V_{1V2v})
2. 1V and 2w (V_{1V2w})



$\mathbf{V_{1V2v} = V_{1V2w}}$

Dyn1

- Connect 1U and 2u
- Keep the neutral floating
- Apply 3Φ Voltage in HV side

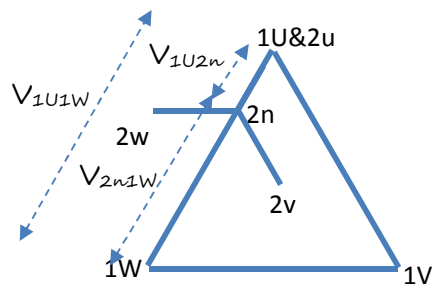


Condition - 1

Measure Voltage between

1. 1U and 2n (V_{1U2n})
2. 2n and 1W (V_{2n1W})
3. 1U and 1W (V_{1U1W})

$\mathbf{V_{1U2n} + V_{2n1W} = V_{1U1W}}$

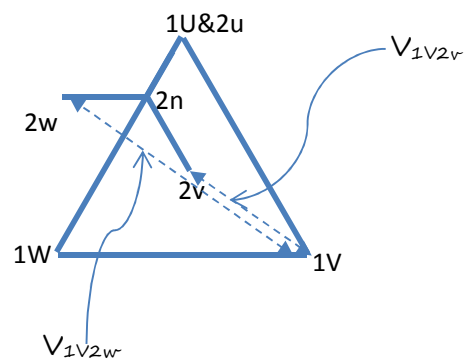


Condition - 2

Measure Voltage between

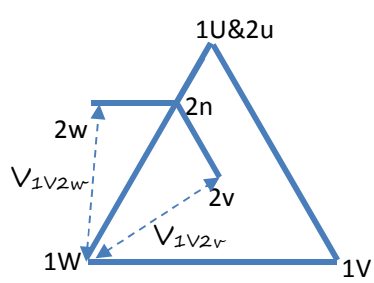
1. 1V and 2v (V_{1V2v})
2. 1V and 2w (V_{1V2w})

$\mathbf{V_{1V2w} > V_{1V2v}}$



Condition -3

Measure Voltage between

1. 1W and 2v (V_{1W2v})
2. 1W and 2w (V_{1W2w})

$\mathbf{V_{1W2v} = V_{1W2w}}$